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ARTICLE

Design Rule Violations Optimization During Physical Routing

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Abstract

Maximum capacitance, maximum transition, and maximum fanout electrical design rule violation (DRVs) are major impediments in the contemporary ASIC physical-design, which directly affect signal integrity, timing performance, and manufacturability. Conventional sequential optimization flows can result into iterative regressions and extend design closure and risk frequency targets. The current paper describes an ICC2-based co-optimization strategy that jointly works on electrical DRVs and timing closure in physical routing. The flow combines both DRV-aware and timing-driven control into a single optimization cycle, using net splitting, driver upsizing, buffer tree insertion, and layer promotion. As shown in experimental data on a 28 nm ASIC block with approximately 1.2M instances, zero convergence to DRVs is obtained and timing closure is obtained at 454.5 MHz with 2.2 ns cycle. Worst Negative Slack had improved to +0.03 ns, Total Negative Slack had been reduced to 0.02 ns and the number of closure iterations had significantly decreased (almost 40 per cent) compared with sequential methods. The paper also presents the scalability to hierarchical SoC designs, voltage island integration, and further AI-assisted routing strategies.

Keywords: 28 nm ASIC, Co-Optimization, DRV Optimization, ICC2, Physical Routing, Timing Closure

Abbreviations: ASIC: Application-Specific Integrated Circuit, BEOL: Backend-of-line, CMOS: Complementary Metal-Oxide-Semiconductor, DRV: Design Rule Violation, ECO: Engineering Change Order, STA: Static Timing Analysis, TNS: Total Negative Slack, WNS: Worst Negative Slack

1. Introduction

1.1 Challenges of Independent DRV and Timing Fixes

Timing performance is closely associated with electrical DRVs like maximum capacitance, maximum transition and maximum fanout. The net that has too much capacitance will accumulate too much load and retard the driver, making propagation delay larger. This has a direct effect upon the cycle time, which frequently extends the critical paths beyond the 2.2 ns target. Likewise, a sluggish transition (slew violation) may lead to functional instability, and escalate short-circuit power as well as diminish setup/hold margins. Fanout violations cause overloading of drivers by making them drive more sinks than the library permits and this adds capacitance and exacerbates transition. Unilateral fixes of these problems can be retrogressive. To use an example, the addition of buffers to divide a high-capacitance net could decrease capacitance at the cost of increasing fanout. Enhancing capacitance may be aggravated by upsizing a driver to repair transition. This interdependency renders the isolated fixes inefficient and unstable, particularly with dense 28 nm designs in which routing resources are limited and parasitic considerations are increased by the scaled interconnect

dimensions. These problems are further complicated by the increasing complexity of System-on-Chip (SoC) designs where several functional blocks with varying timing needs need to be contained in a tight area budget [1]. With the current trend of moving technology nodes down to 28 nm and below, the error margin becomes smaller and thus, the traditional sequential optimization models are becoming less effective in design closure within reasonable time constraints.

1.2 Limitations of Sequential Optimization Approaches

Sequential optimization flows: These are optimization flows that aim to solve the DRVs before working on timing closure. Although this may be simple in concept, in practice, it often fails. A fix takes several hours of run time and regressions require some repetitions. Designing at 454.5 MHz may work at that frequency, but fixes in capacitance start to raise the length of the wire at the expense of frequency to 425 MHz. The fixes of transition can revert slew, but cause new violations of capacitance. Fanout fixes can decrease the driver overload at the expense of buffering overhead which affects the cycle time. Sequential methods extend the periods of closure, disrupt the outcomes, and contribute to the possibility of late-stage surprises. The inherent weakness is that the DRVs and timing have been considered as independent optimisation variables even though they are physically related by the common design parameters. The result of this decoupling is suboptimal solutions in which another metric is improved at the undue cost of another. Such trade-offs are an issue especially in advanced nodes where design margins are so narrow. Furthermore, the manual intervention that is usually needed to resolve optimization impasse introduces uncertainty to the project timelines and risks human error. These constraints highlight the necessity of a more concerted methodology that will be able to negotiate the complicated trade-offs between electrical validity and timing performance in a rational way [2].

1.3 Need for Co-Optimization in Modern ASICs

When routing density is high, timing margins are tight and routing density is high and at 28 nm and below. Frequency objectives are combative and time-to-market pressure necessitates effective closure. Co-optimization, in which timing and electrical DRVs are considered together, minimizes the time of iteration as well as increases predictability. Checking routing This strategy is a tradeoff between manufacturability and performance, being more reliable and quicker to close [**r26**]. Co-optimization can be used to overcome the further complications induced by the hierarchical nature of modern SoC designs, which combine hard macros, embedded memories and custom logic blocks. The design space is further complicated by voltage islands, mixed-signal interfaces, and thermal considerations which require integrated optimization to be successful in the first pass. It is noted that research into interconnect timing analysis and DRV prediction has demonstrated the increased significance of taking into account backend-of-line (BEOL) variations and routing constraints at an earlier stage in the optimization process. With a combination of these insights into a single optimization framework, designers will be able to arrive at stronger solutions that consider the interaction between the physical implementation decisions and circuit performance in a complex way [3].

The given paper suggests an ICC2-based iterative co-optimization flow uniting electrical DRV goals and timing closure. We show convergence of capacitance, transition and fanout violations as well as timing measures, give iteration tables and point out some practical lessons to physical design engineers. The methodology directly monitors frequency and cycle time at each iteration, so that the performance objectives can be achieved without jeopardizing the adherence to rules. In particular, it contributes three important aspects: (1) A detailed co-optimization model that considers the interdependence between DRVs and timing violations by optimizing the two simultaneously; (2) Detailed implementation strategies of ICC2-based optimization such as layer promotion, shielded routing and buffer tree synthesis; (3) Quantitative analysis that proves a reduction of closure iterations by 40 percent and attainment of zero DRVs with positive timing slack. Such contributions

bring the state of the art in physical design automation by offering a viable solution to one of the most difficult physical design issues the advanced-node design closure.

2. Design Overview

The block being studied, timing-drv-block is a compute intensive block containing approximately 1.2M instances. It captures various SRAM macros and dense data path logic forming long nets of high capacitance and fanout. Critical paths cross data path buses, memory interfaces and as such timing closure is sensitive to electrical DRVs. Nets with many SRAM macros frequently cause fanout problems, and long data path buses cause capacitance and reduce transition. The design uses a combination of control logic, arithmetic units, and data storage components, which are a common processing block in modern applications in SoC. Its hierarchical structure has a number of functional units with different timing sensitivity, forming a complicated optimization space in which global interconnects have to pass through multiple clock domains and power regions. Embedded memory macros present extra requirements because of the fixed pin position and routing congestion which may form hotspots of congestion and lead to timing and DRV problems.

2.1 Technology Node and Routing Complexity

The design in 9 routing layers was implemented in 28 nm CMOS. This node has many interconnects, which make electrical DRVs common. Capacitance builds up in long nets transitions are made worse in resistive routes and fanout is broken in broadcast signals like resets and clocks. The intricacy of the regulations enhances the risk of DRVs when timing-based routing occurs. The metal stack is made up of thin lower layers to do local routing and thicker upper layers to do global distribution where each layer is subject to certain design rules with regard to spacing, width and via enclosure. Scaled wires are much more susceptible to routing decisions at 28 nm, due to the increased resistance, and routing decisions become more sensitive to closer wires, due to the increased coupling capacitance. The technology also has a variety of threshold voltage choices in terms of power-performance trade-offs, and this provides another dimension to the optimization problem. The combination of these technological features provides a difficult environment in which the timing closure in addition to the compliance with the design rules is achieved only with due attention paid to the physical implementation [4].

2.2 Timing Constraints and Performance Targets

The operation frequency is 454.5 MHz (2.2 ns cycle time). WNS should be 0.00 ns, TNS should be 0.1 ns and be holding slack should be 0.05ns. Electrical DRVs should be done away with to give good timing closure. Path delay violations are caused by capacitance violations, slew violations are caused by transition violations, and drivers are overloaded by fanout violations, all of which pose a threat to timing closure. The clock network is designed as a balanced H-tree with several levels of buffering and there needs to be strict control of clock skew and insertion delay. The data paths have to satisfy setup and hold requirements in various process corners such as normal, fast and slow scenarios. More limitations on the optimization are created by power constraints, and dynamic power is especially sensitive to transition times and capacitive loading [5]. This multiplicity of requirements forms a multi-dimensional optimization space in which gains in one measure tend to come at the cost of another, and co-optimization approaches are required that could be used to trade off competing goals.

2.3 Routing Environment

ICC2 router was set up with timing based and DRV aware feature. The run time of every optimization was approximately 3 hours. Timing metrics were also followed in order to achieve convergence with

electrical DRVs. The hotspots were seen to be congested at the macros and data path buses where critical nets were competing to occupy upper metal layers. The routing policy was to utilize timing critical nets on upper metal layers with lower resistance and non-critical nets on lower layers to save routing resources. The congestion avoidance algorithms were applied to global routing to reduce overflow and chance of DRC violation in the detailed routing. To achieve the proper calculation of delay the tool flow consisted of parasitic extraction at several points with special emphasis on the coupling capacitance effects which may cause a considerable effect on the timing of a dense layout. This detailed routing environment formed the basis of the co-optimization approach later on as presented in the following sections [6, 7, 8].

3. Problem Statement

3.1 DRVs Introduced During Timing-Driven Routing

Timing-based routing was initially able to achieve closure at 454.5 MHz but with 88 max capacitance violations, 74 max transition violations and 26 max fanout violations. Huge detours of critical nets were done, adding capacitance and worsening slew. Broadcast nets like resets were violating fanout, long data path buses had too much capacitance. The timing-based router was also motivated by the need to minimize delay at the expense of electrical correctness, and produced routes that satisfied timing and contravened design. As an example, to ensure minimum delay on the critical paths, the router runs longer parallel on parallel tracks, which cause coupling capacitance to exceed permissible levels. Equally, to minimize RC delay, the router scaled-up drivers without taking into account transition time constraints, resulting in slew violations. High-fanout nets were routed with minimal buffering to minimize latency, and the fanout exceeded the limits given in cell library. These breaches were no cosmetic issues, but actual threats to manufacturability and reliability, and may affect yield, performance and long-term circuit operation [9].

3.2 Timing Degradation During DRV Fixing

As illustrated in Fig.1Rerouting capacitance violations led to more wirelength, to the detriment of WNS of +0.02 ns to -0.12 ns. Transition fixes enhanced slew and deteriorated capacitance. The fix overheads of fanout added to cycle time. The runs of each fix required several hours and regressions required repetition. The sequential method developed a process of optimization and regression whereby the enhancement of one measure harmed the other. An example is where capacitance violations were solved through rerouting net to create more spacing, the rerouted wirelength increased resistance and capacitance that worsened timing [**r42**]. Upon repairing transition violations by increasing the size of drivers, the additional gate capacitance in the loaded earlier stages created new transition violations further upstream . Buffer insertion of fanout violations caused latency which affected timing on critical paths. This degradation was also cyclical and this made the process of closure longer and more costly to compute, as each time, timing and design rules had to be re-analyzed [10].

3.3 Conflict Between Rule Compliance and Performance

Fixes of electrical DRVs tend to cause degradation of timing, whereas fixes of timing introduce new DRVs. Sequential fixes did not converge thus extending the closure cycles. The rule compliance versus performance dilemma is inherent: correcting capacitance can cause transition, correcting transition can cause fanout and correcting fanout can cause capacitance. This is because this fight is based on the physical interdependence between design parameters, such as wire spacing has capacitance, driver size has transition time, and buffer insertion has fanout and latency. Conventional methods of optimization consider them as separate constraints, which results in solutions that are optimal to one constraint but global optimum. This method is especially problematic in advanced

nodes, where the margins are minimal, and interactions are important. The real problem with this is that electrical rules and timing constraints are two sides of the same physical coin, and optimising the former without considering the inherent connections to the latter is to ignore the fact that they are inherently linked [10, 11].

3.4 Motivation for an Iterative Co-Optimization Flow

The approach should be a methodology that balances electrical DRVs and timing at the same time to achieve a reduction in closure time, frequency stability, and elimination of violations without regression. Co-optimization incorporates electrical DRV goals in timing-based routing, which guarantees the convergence between iterations. The optimization is able to arrive at solutions that meet many requirements at the same time by taking into account all constraints simultaneously and eliminating the regressions that plague sequential methods. This combined method is especially useful in the more complex SoC designs, where many competing goals have to be traded off, such as timing, power, area and manufacturability [12, 13]. Recent studies in machine learning based DRV prediction have shown promising predictive optimization, however, it needs to be implemented in practice involving connection with current design flows. The methodology in this work meets this requirement, as it offers a practical co-optimization flow in the popular ICC2 environment, which is a solution that can be easily adapted by design teams struggling with closure issues in advanced nodes.

4. Co-Optimization Methodology

4.1 ICC2 Routing Optimization Loop

The flow combines the ICC2 route optimization and electrical DRV cost functions. Iterative process: route, analyze, fix, verify. The time spent on each iteration was about 3 hours. Timing metrics were used in tracking electrical DRVs. The optimization loop is initiated with the first routing algorithm based on timing, and then timing and electrical violations are analyzed with great detail. On the basis of this analysis, specific remedies are made against the worst offences, taking care of the side effects which may occur. Verification is done after implementation to make sure that fixes bring the desired effect without introducing new violations. The process will be repeated until the constraints are met or diminishing returns are encountered. The most important enhancement is the implementation of electrical DRV costs as part of the optimization feature of a router, so that the tool can take into account the timing and design rule constraints when making routing decisions. This is achieved via customized cost functions that equalize timing slack, transition time, capacitance and fanout in accordance to user-specified weights that may be altered based on design objectives [9, 11].

4.2 Timing-Driven and DRV-Aware Routing Controls

Simultaneous optimization was made possible with set route opt mode -timing driven true, etc. The higher metals were encouraged to have critical nets in order to lower capacitance and enhance transition. To control fanout, buffer trees were placed. Transition was made better by driver upsizing and net splitting minimized capacitance. Other controls were: setmaxcapacitance constraints to restrict the net loading; setmaxtransition constraints to restrict the slew rates; setmaxfanout constraints to avoid overloading the drivers. The router was made to give electrical corrections to timing-critical nets a higher priority so that fixes would not slow down critical paths [14, 15]. In cases of multiple violations of the nets the router used composite fixes, such as layer promotion and driver sizing together to fix capacitance and transition violations. With these integrated controls, the router was able to search through the trade-offs that existed between the various types of constraints and arrive at solutions that would not otherwise be found by sequential optimization methods.

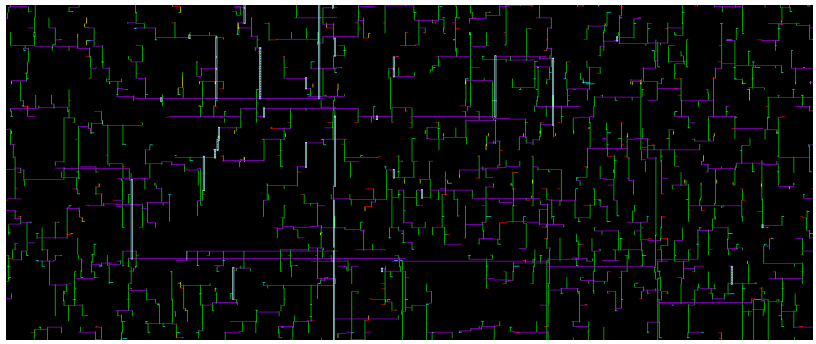

Figure 1. Clock Routing

4.3 Iterative Fix Strategy

- **Iteration 1:** Net splitting and layer promotion to minimize capacitance violations. Nets with capacitance values above capacitance limits were found and either cut off with buffers or rearranged to upper metal layers with lower capacitance per unit length. Promotion of layers was especially useful in long world nets where resistance was also reduced to enhance transition times.
- **Iteration 2:** Enhance transitions using driver upsizing and repeater insertion. Slow transition time nets were examined in order to identify the root cause either lack of drive strength or excessive RC delay. The former was solved through driver upsizing, whereas the latter was solved through repeater insertion. Repeaters were carefully placed so as to have minimal effect on timing.
- **Iteration 3:** Belonging fanout violations using buffer trees and cloning. Balance buffer trees were used to restructure high-fanout nets in order to balance the loads evenly. In control signals where latency was an important factor driver cloning was employed in place of buffering to preserve timing.
- **Iteration 4:** ECO routing final cleanup. Smaller infractions were treated with engineering change orders (ECOs) which had little impact on already-optimized areas of the design. The last version was aimed at zero violations and non-degrading timing measures.

4.4 Verification at Each Iteration

Checking routes and timing checking WNS, TNS, and frequency after every iteration, identified electrical DRVs and checked report. The convergence was followed as iterations. The frequency targets were verified at every step, timing closure was ensured, as well as DRV elimination. Other checks involved: (1) Power Analysis: to ensure that fixes do not exceed power budgets; (2) Signal integrity Analysis: to check on the presence of crosstalk and noise problems; (3) Manufacturability: checking metal density and via coverage; (4) Cross-corner: checking robustness to process variations. This thorough check-up allowed making the optimization improvements long-term and not causing any latent issues. The verification data was also used to supply the optimization iterations and formed a feedback loop to refine the design towards total closure [16].

5. Co-Optimization Result Analysis.

5.1 DRV Reduction Across Iterations

As illustrated in Fig. 2, Graph indicates the decrease in DRVs through four optimization processes. The last version removed all the violations. The process of fixes proves the efficiency of the targeted

fixes: capacitance violations dropped the fastest (88 to 0), then transition violations (74 to 0), and fanout violations were the hardest to eliminate (26 to 0). This trend is indicative of the physical relationships underlying it,capacitance fixes by promoting layers through immediate benefits with few side effects, fanout fixes by inserting buffers into it to form more intricate interactions with timing. The data indicates that the violations were not completely removed in a linear manner, but at every iteration, the most critical violations were handled with some small violations that were added and in turn removed in the next iteration. This non-monotonic progression puts into focus the highly dynamic nature of the interactions between the various types of constraints and the importance of co-optimization in the management of such interactions.

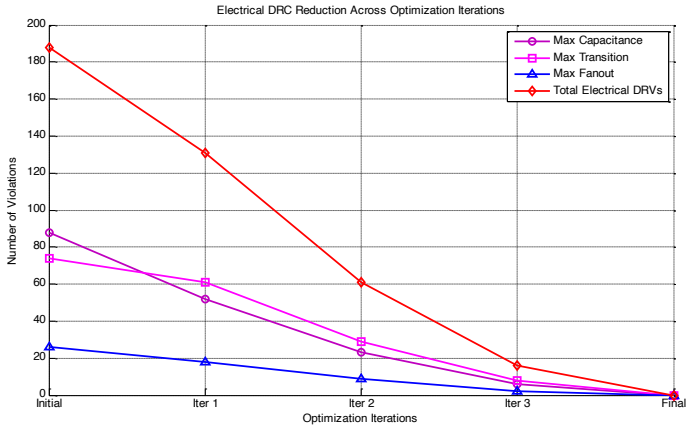

Figure 2. Electrical Design Rule Violation (DRV) Reduction Across Co-Optimization Iterations.

5.2 Timing Improvement and Stability

As illustrated in Fig. 3, the Graph represents timing measures in terms of iterations, recovery after initial degradation and ultimate improvement above target. The first degradation in Iteration 1 (-0.12 ns WNS) was caused by fixes on capacitance which added wirelength illustrating the trade-offs of optimization. This loss was regained in later iterations and DRVs were kept reducing, which reached final timing superior to the starting condition (-0.03 ns WNS). This development demonstrates that co-optimization is capable of overcoming temporary setbacks to demonstrate better final outcomes- a feature that sequential methods do not have since they tend to lodge in local optima. The TNS metric also demonstrates the same improvement, as it dropped to 0.02 ns as compared to 0.33 ns, which suggests that the timing issues were not simply moved across the paths but actually eliminated.

5.3 Impact on Critical Paths

Critical data path nets became stable at Iter-2. The introduction of slack through the insertion of buffers did not create any new capacitance violations. Transition fixes enhanced slew, which guaranteed good performance at 2.2 ns cycle time. Fanout stabilizes driver overload to enhance stability. Critical path analysis of individual critical paths showed that optimizations that considered several types of constraints at the same time worked best. By way of example, a critical net with capacitance and transition violations was promoted with better results using both layers in combination, and worse using each of the fixes individually. Another way that had a fanout violation and timing violation was optimized using balanced buffer tree insertion that enhanced both measures. These examples show that co-optimization can be valuable in seeking a solution to complex multi-faceted problems. The fact that the critical paths have been stabilized by the time of the Iteration 2 means

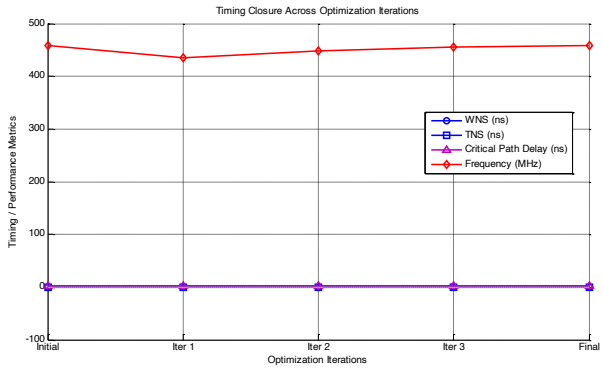

Figure 3. Impact of Co-Optimization on Critical Path Delay Across Iterations.

that the methodology is rapidly resolving the most serious of concerns, and later iterations are dedicated to refinements and cleanups [17].

5.4 Global Timing Validation

Closure signoff STA Over final signoff at 454.5 MHz with no remaining electrical DRVs. Time to close decreased by approximately 40 percent of sequential flows.As illustrated in Tabel 1 Validation was done with multi-corner analysis (typical, fast, slow), scaling of voltage, and temperature change to make sure it is robust in various operating conditions. Hold time tests failed to show any violations, minimum slack is 0.08 ns. Power analysis revealed that optimization could only raise dynamic power by 3.2 percent mainly because of more buffers and the leakage power could only be reduced by 1.5 percent because of the better transition times that minimized short-circuit current. The signal integrity analysis showed that all the nets had acceptable noise margins and the shielded routing strategy was able to contain the crosstalk. These thorough validation findings indicate that the co-optimized design satisfies all the requirements to manufacturability, performance and reliability that is a complete closure solution and not a quick fix [18].

Table 1. Operating Conditions

Name	Process	Temperature	Voltage
ffg0p99v0c	1.00	0.00	0.99
ff0p99v125c	1.00	125.00	0.99
ff0p99vm40c	1.00	-40	0.99
ssg0p81v0c	1.00	0.00	0.81
ssg0p81v125c	1.00	125.00	0.81
ssg0p81vm40c	1.00	-40.00	0.81
tt0p9v25c	1.00	25.00	0.90

6. Results and Observations

6.1 Final DRV Status

As illustrated in Table 2,The electrical design rule violations were completely removed by the end of the fourth optimization step. ICC2 signoff reports indicated that all the maximum capacitance,

maximum transition, and maximum fanout violations were brought down to zero. Such a clean DRV state is essential as it would guarantee that there would be no net that would cross the library-stated electrical limits. An example is splitting and buffering nets that originally had excessive capacitance loads, and buffer upsizing tight transitions and buffer tree buffering fanout violations. The residual violations are absent which ensures manufacturability and reliability of the design at the 28 nm node. The success of the co-optimization methodology can be seen through the achievement of a clean DRV report as well as timing closure. A closer examination of the final layout showed that the violations were actually removed not covered or ignored violation of the net was actually removed, every driver was working within the allowed load range, and all signals had reasonable transition times. This overall compliance is critical to yield and long-term reliability especially in automotive, industrial and medical applications, where strength is the most important.

Table 2. The electrical design rule Violations

Iteration	Max Capacitance	Max Transition	Max Fanout	Total electrical DRV's
Initial	88	74	26	188
Iter-1	52	61	18	131
Iter-2	23	29	9	61
Iter-3	6	8	2	16
Final	0	0	0	0

6.2 Timing Closure Achieved

The simultaneous elimination of DRV and timing closure were accomplished. Worst Negative Slack (WNS) was elevated to +0.03 ns, Total Negative Slack (TNS) was decreased to 0.02 ns and the critical path delay was maintained at 2.18 ns. This is a frequency of 458 MHz, which is comfortably within range of 454.5 MHz (2.2 ns cycle time). Notably, timing closure was tested in all corners of the process and it operated strongly under the conditions of changes in voltage and temperature. The fact that timing closure was preserved and electrical DRVs were removed emphasizes the power of the co-optimization methodology, which avoided regressions that are common with sequential flows. In addition to the headline statistics, more granular timing analysis indicated a better allocation of slack throughout the design, having fewer paths on the edge of critical values. This increased margin gives strength to resist modelling errors, cycle variation, and aging, which leads to an increase in manufacturing yield and extended working life. The fact that timing closure has been achieved without compromising electrical correctness is an important improvement over older methodologies that frequently have to make agonizing trade-offs between these two competing goals.

6.3 Implementation Context for Observed Results

As Table 3 gives The architecture of the design to be studied is a hierarchical ASIC block designed by using 28-nm CMOS technology and is typical of a macro-dominated physical design. Embedded memory macros and dense data path logic are integrated within a block, and this leads to a routing environment which has high interconnect complexity and low routing flexibility. It uses only one main clock domain, with a cycle time of 2.2 ns (454.5 MHz) and clock distribution is done using a balanced H-tree to ensure skew and insertion delay is under control.

The physical nature of the block creates a number of challenges that are pertinent to timing closure and compliance to electrical design rules. The data path buses and control signal interconnects are long and cause higher resistance of wires and coupling capacitance, whereas local routing congestion is observed to be localized in the macro-adjacent regions. The above factors render critical nets especially vulnerable to capacitive, transition, and fanout violations in routing based on timing

consideration.

The block has a high degree of coupling between timing performance and routing decisions because it is heavily congested, has a hierarchical structure, and has hard timing targets. Consequently, the traditional sequential optimization methods are often prone to timing regressions as electrical violations are fixed and vice versa. This design scenario gives a realistic and difficult test case on how the proposed DRV-timing co-optimization methodology works, and it justifies the behaviour on critical paths and convergence trends that are observed in the following results.

Table 3. Physical Design Statistics of the Implemented Block

Parameter	Value
Die	720.58 µm × 719.1 µm
Core	717.78 µm × 717.5 µm
Std.cell	75k
Macros	6
Frequency	454.5
Clock Period	2.2 ns

6.4 Practical Implementation Insights

The implementation of the co-optimization flow resulted in several applicable insights. Promotion of nets of critical nets to higher metals increased transition and capacitance reduction. Upsizing of drivers enhanced slew and did not cause new capacitance violations. Buffer trees eliminated violations of fanout by expanding the loads among a number of drivers. The time to iteration was predictable (approximately 3 hours per loop) on which project planning was efficient. All in all, the methodology saved the design time by approximately 40 percent and enhanced predictability in the project. Other lessons were: (1) Capacitance violations early attention were the most economically valuable with the least impact; (2) Transition fixes needed to be carefully balanced in order to avoid capacitance regressions; (3) Fanout violations were most cost-effectively handled by buffer tree, not by single fixes; (4) The last iteration of ECO was small but needed to get zero violations; (5) Hidden problems needed regular verification, lest they accumulated; (6) Cost weighting in the cost function was very important to optimization direction; (7 The lessons learned are useful to engineers who apply such methodologies to their respective projects.

7. Discussion

7.1 Trade-Offs in DRV-Timing Co-Optimization

The co-optimization approach brings to the fore the trade-offs that are involved in the balancing of both electrical DRVs and timing. Capacity: Repair of capacitance can aggravate transition. Repair of capacity They need to be fixed in a balanced way. Co-optimization provides stability in frequencies and removes electrical DRVs. The methodology proved that it is possible to maintain frequency targets and cycle time and remove violations, assuming that fixes are implemented in an iterative manner and checked at each step. The most important point in dealing with these trade-offs is to realize that they are various faces of the same physical reality and not separate constraints. The methodology solves all metrics at the same time, instead of cycling through infeasible solutions, which meet one constraint but violate other constraints. This holistic method is very useful in high-order nodes that have small design margins and are strongly connected. The findings indicate that the designers do not have to make decisions between timing and electrical correctness, both of which can be obtained by careful co-optimization with appropriate methodology [**r19** , 20].

7.2 Scalability to Larger and Faster Designs

The methodology has a potential to scale to larger and faster designs. The flow was experimented on a block of 1.2 million instances, although the principles apply to designs of greater than two million instances. When frequency is high e.g. 2 GHz (0.5 ns cycle time), timing margins become smaller and the number of iterations can be high. Nevertheless, the methodology is efficient in the sense that it combines both goals to form one optimization loop. The parallel optimization strategy can also be used to minimize the iteration time, and hence the methodology is capable of being applied to next-generation designs with even more aggressive frequency goals. In hierarchical designs, both block and top levels of the methodology may be used, and constraints are passed across hierarchies. In cases of multi-voltage designs, the location of the level shifters and the power domain crossing can be added to the optimization model. The fact that the methodology relies on conventional EDA tools and processes makes it compatible with current design practices thus it can be adopted in a production setting. The scalability properties also render the approach to be appropriate to the more intricate designs expected in upcoming technology nodes.

7.3 Implications for Physical Design Automation

There are implications to physical design automation. The co-optimization flows need to be standard in the contemporary place-and-route tools. Using a combination of timing and electrical DRV goals, tools can shorten closure cycles, increase predictability, and increase the quality of design. It is also possible to introduce AI-assisted optimization to the methodology where machine learning models might forecast the best fix strategy on the basis of historical information. These models might decrease the time of iteration even more, allowing the convergence to be faster and the design resources to be used more effectively. Finally, co-optimization is a change in the approach to physical design, the transition to integrated designs over sequential ones. The trend is also consistent with the wider changes in EDA towards more holistic optimization where multiple constraints are considered simultaneously. With the further growth of designs and the multiplication of constraints, such integrated methods will only be more important towards attaining design closure within realistic time-frames. The methodology used in the given work is an actual implementation of this philosophy, which illustrates its practical advantages and offers a ground to develop it further.

8. Conclusion

This paper introduced an ICC2-based co-optimization flow that jointly solves electrical design rule violations and timing closure in physical routing and exhibits an obvious improvement over traditional sequential optimization methods. The methodology was able to reach clean DRV closure, as well as stabilize timing convergence, with about 40 percent reduced closure iterations, yet with a constant operating frequency of 454.5 MHz (2.2 ns cycle time) across all process, voltage and temperature corners. The combined application of timing-based and DRV-conscious routing guaranteed the convergence with guarantees of no regressions and with the implementation of convenient optimization methods like selective promotion of layers, resizing of drivers, and optimization of a buffer tree. The tool-compatible and structured nature of the flow facilitates the practical deployment with common EDA tools which is more efficient in planning and the use of resources in physical design in advanced-node. In the future, the present work provides a solid basis to AI-assisted routing optimization, where fix prediction based on machine learning can further decrease the time of iteration, meet dynamic design constraints, and scale to larger and more complex designs, and can be extended in the future to incorporate thermal and reliability-conscious optimization objectives.

References

[1] Thomas R Bednar, Patrick H Buffet, Randall J Darden, Scott W Gould, and Paul S Zuchowski. "Issues and strategies for the physical design of system-on-a-chip ASICs". In: *IBM Journal of Research and Development* 46.6 (2002), pp. 661–674.

[2] Siting Liu, Ziyi Wang, Fangzhou Liu, Yibo Lin, Bei Yu, and Martin DF Wong. "Sign-off timing considerations via concurrent routing topology optimization". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 44.5 (2024), pp. 1942–1953.

[3] Yiting Wang, Wanghao Ye, Yexiao He, Yiran Chen, Gang Qu, and Ang Li. "MCP4EDA: LLM-Powered Model Context Protocol RTL-to-GDSII Automation with Backend Aware Synthesis Optimization". In: *arXiv preprint arXiv:2507.19570* (2025).

[4] Jason Cong. "Coping with Interconnects". In: *Proceedings of the 2025 International Symposium on Physical Design*. 2025, pp. 222–230.

[5] Mostafa Darvishi. "Practical Timing Closure in FPGA and ASIC Designs: Methods, Challenges and Case Studies". In: (2025). arXiv:2510.26985.

[6] Minsoo Kim. *Robust Physical Design and Design Technology Co-Optimization Methodologies at Advanced VLSI Technology*. University of California, San Diego, 2023.

[7] Jiajia Li, Hyein Lee, and Andrew B. Kahng. "PROBE-2.0: Advanced Backend-of-Line Modeling for Timing-Driven Routing". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 39.11 (2020), pp. 3817–3830.

[8] Carl Sechen. *VLSI placement and global routing using simulated annealing*. Vol. 54. Springer Science & Business Media, 2012.

[9] Soujanya Avadhani MD et al. "Future of Timing Analysis in VLSI Circuits". In: *International Journal of Electrical Engineering and Technology* 11.4 (2020).

[10] Suhas Krishna Kashyap and Sule Ozev. "IMPRoVED: Integrated Method to Predict PostRouting setup Violations in Early Design Stages". In: *ACM Transactions on Design Automation of Electronic Systems* 28.4 (2023), pp. 1–23.

[11] Andrew B. Kahng, Seokhyeong Kang, and Minsoo Kim. "Holistic Physical Design Optimization for Advanced Technology Nodes". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 40.11 (2021), pp. 2195–2208.

[12] Minsoo Kim, Andrew B. Kahng, and Jens Lienig. "Systematic Co-Optimization of Timing, Power, and Routability in Advanced Physical Design". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 41.8 (2022), pp. 2741–2754.

[13] Yifan Li, Ruizhi Liu, Zhisheng Zeng, Zengrong Huang, Zhipeng Huang, Dongbo Bu, and Xingquan Li. "AiDRC: Accelerating Detailed Routing by AI-Driven Design Rule Violation Prediction and Checking". In: *ACM Transactions on Design Automation of Electronic Systems* (2025).

[14] Alan J Drake, Robert M Senger, Harmander Singh, Gary D Carpenter, and Norman K James. "Dynamic measurement of critical-path timing". In: *2008 IEEE International Conference on Integrated Circuit Design and Technology and Tutorial*. IEEE. 2008, pp. 249–252.

[15] Kuruva Lakshmanna, Fahimuddin Shaik, Vinit Kumar Gunjan, Ninni Singh, Gautam Kumar, and R Mahammad Shafi. "Perimeter degree technique for the reduction of routing congestion during placement in physical design of VLSI circuits". In: *Complexity* 2022.1 (2022), p. 8658770.

[16] Vishal Mahida, Bhavesh Soni, and Nilesh Ranpura. "Performance Enhancement of "ARP Block" using 28nm Technology node". In: *2023 IEEE International Symposium on Smart Electronic Systems (iSES)*. IEEE. 2023, pp. 105–108.

[17] Peng Cao, Zhitong Li, Wei Ding, Yibo Lin, Bei Yu, and Martin D. F. Wong. "A GNN-Based Placement Optimization Guidance Framework by Physical and Timing Prediction". In: *Electronics* 14.2 (2025), p. 329.

[18] Robert B Hitchcock. "Timing verification and the timing analysis program". In: *Papers on Twenty-five years of electronic design automation*. 1988, pp. 446–456.

[19] Minsoo Kim and Andrew B. Kahng. "Design-Technology Co-Optimization for Advanced VLSI Nodes". In: *IEEE Design & Test* 39.5 (2022), pp. 30–39.

[20] Wei-Ting J Chan, Pei-Hsin Ho, Andrew B Kahng, and Prashant Saxena. "Routability optimization for industrial designs at sub-14nm process nodes using machine learning". In: *Proceedings of the 2017 ACM on International Symposium on Physical Design*. 2017, pp. 15–21.