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ARTICLE

# Revolutionizing CMOS VLSI with Innovative Memory Design Techniques

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**Abstract**

The revolution in CMOS VLSI (Complementary Metal-Oxide-Semiconductor Very-Large-Scale Integration) technology is being driven by innovative memory design techniques that address the ever-growing demand for faster, smaller, and more power-efficient devices. Traditional memory architectures are being reimagined to overcome limitations in speed, density, and energy consumption. Techniques such as multi-level cell (MLC) storage, resistive RAM (ReRAM), and spin-transfer torque magnetic RAM (STT-MRAM) are at the forefront of this transformation, offering significant improvements over conventional SRAM and DRAM technologies. MLC storage increases memory density by storing multiple bits per cell, while ReRAM and STT-MRAM leverage novel materials and mechanisms to enhance speed and reduce power usage. These advancements are critical for applications ranging from high-performance computing to portable electronics, where memory performance directly impacts overall system efficiency and capability. Furthermore, integration of 3D memory stacking and neuromorphic computing architectures is paving the way for future developments, enabling even greater data processing capabilities within compact form factors. The adoption of these cutting-edge memory design techniques in CMOS VLSI not only pushes the boundaries of current technology but also sets the stage for the next generation of electronic devices. As these innovations continue to mature, they promise to revolutionize the landscape of memory technology, driving unprecedented advancements in computing and electronic systems.

**Keywords:** Multi-Level Cell (MLC) Storage; Resistive RAM (ReRAM); Spin-Transfer Torque Magnetic RAM (STT-MRAM); VLSI Technology; 3D Memory Stacking

**Abbreviations:** ABB: Adaptive body biasing, BTI: Bias Temperature Instability, BIST: Built-in self-test, CNT: Carbon Nanotube, DTCO: Design Technology Co-Optimization, DVFS: Dynamic Voltage and Frequency Scaling, ECC: Error-Correcting Code, PCM: Phase Change Memory, PUF: Physical Unclonable Function, SSTA: Statistical Static Timing Analysis, SoC: system-on-chip, STCO: System-technology co-optimization, TRNG: True Random Number Generator

## 1. Introduction

The electronics industry has continuously enhanced circuit performance while keeping costs stable through the scaling of transistor dimensions, a trend known as Moore's law. However, this scaling approach faces challenges at sub-30nm and sub-10nm technology nodes, prompting the exploration of alternative solutions like FinFETs and Fully Depleted Silicon On Insulator (FDSOI) transistors. As technology progresses, process costs and electrical issues hinder the profitability of these solutions, necessitating enhanced transistor functionality rather than mere dimensional scaling. A promising functionality-enhanced device is the Silicon NanoWire Field Effect Transistor (SiNWFET), offering dynamic control over majority carrier type, subthreshold slope, and threshold voltage. These capa-

bilities enable denser logic gates using fewer transistors than equivalent CMOS gates. Memories, including SRAM, DRAM, and non-volatile options like flash, are crucial VLSI building blocks known for their dense, regular wiring. This article explores innovative memory design techniques revolutionizing CMOS VLSI, covering aspects like memory cell design, array organization, sense amplifiers, design shift left, digitization, reliability challenges, solutions, and design technology co-optimization [1, 2].

## 2. Memory Cell Design

The most prevalent memory cell used today is the 6T SRAM cell. It comprises six transistors, one wordline, and two bitlines for read and write operations. The read operation involves precharging both bitlines high, and the cell pulls one line low. For writing, one bitline is forced low while the other remains high, overpowering the pull-up pMOS. To ensure proper functionality, the nMOS pull-down transistor should be 1.5-2x wider than the pMOS pull-up 1.

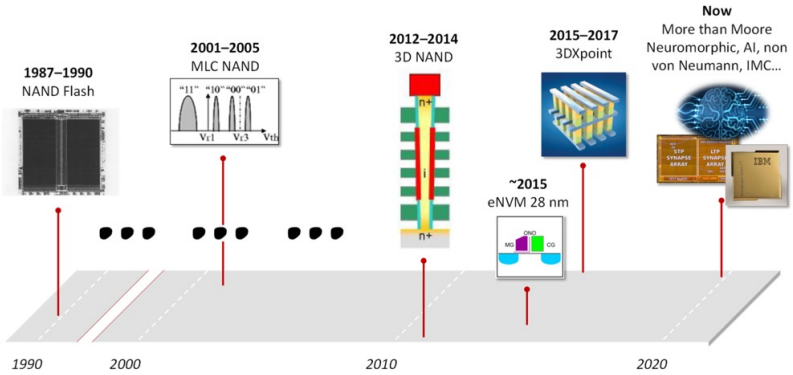


**Figure 1.** Main milestones in the history of nonvolatile memories.

SRAM arrays employ decoders to select a single cell on each set of bitlines, disconnecting unselected cells. Bitline I/O circuits, precharging, and qualified wordline signals facilitate reading and writing while avoiding conflicts. Write drivers must have sufficiently low resistance to properly write the cell. Bitline multiplexing is commonly used to share I/O circuits across multiple bitlines. Sense amplifiers can detect smaller bitline signals for faster access times in large arrays [3, 4].

This chapter explores the use of SiNWFETs in memory designs, focusing on two main categories:

- **Volatile Memory (e.g., SRAM, DRAM, flip-flops)**: Innovative SiNWFET-based True Single Phase Clock (TSPC) flip-flops with embedded asynchronous set, reset, and logic operations are proposed. These SiNWFET TSPC flip-flops exhibit:
  - 20% area reduction
  - 30% delay reduction
  - 7% leakage power reduction compared to CMOS-based TSPC flip-flops.
- **Non-volatile Memory (e.g., RRAM)**: SiNWFETs are explored as selectors in 1-Transistor 1-RRAM (1T1R) bitcells. Two SiNWFET-based bitcell designs, 1PCT1R and 1XPCT1R, leverage dynamic polarity control to enable low-voltage operation and improve density compared to CMOS-based 2T1R bitcells.

## 3. Memory Array Organization

Memory arrays are organized into rows and columns, with each cell located at the intersection of a wordline (row) and a pair of bitlines (columns). Decoders are used to select a specific wordline and bitline pair, enabling access to the desired memory cell [5, 6] (see Fig. 2).

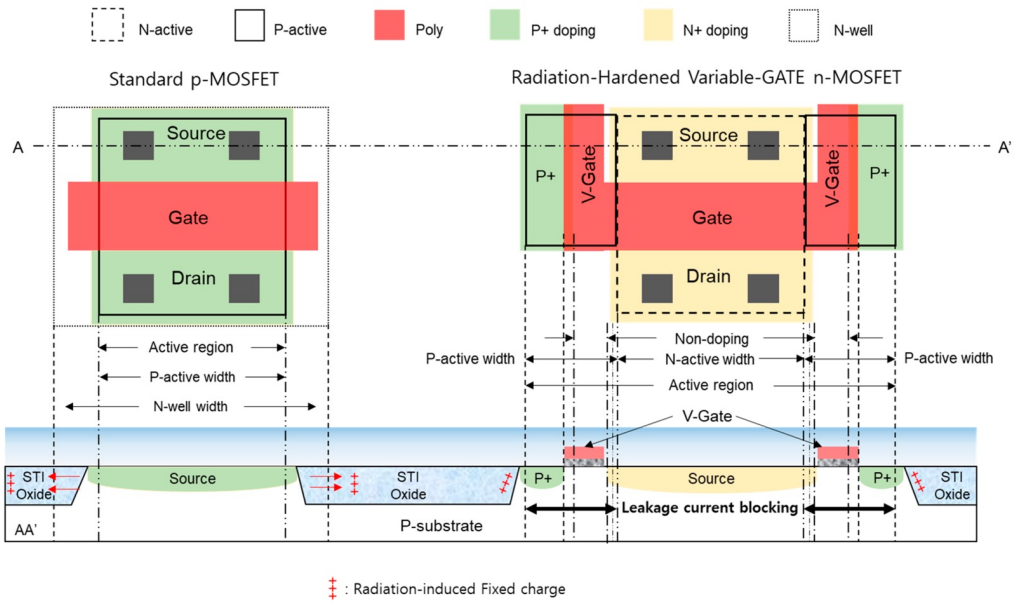


**Figure 2.** Basic configuration of the proposed RH CMOS logic circuit.

1. **Wordline Decoder**: This circuit decodes the row address and activates the corresponding wordline, connecting the cells in that row to the bitlines.
2. **Bitline Organization**:
   - Bitlines run vertically and are organized in pairs (bitline and bitline_bar) to transfer data during read and write operations.
   - Bitline multiplexers are often employed to share sense amplifiers and write drivers across multiple bitline pairs, reducing area overhead.
3. **Sense Amplifiers and Write Drivers**:
   - Sense amplifiers detect and amplify the small voltage differences on the bitlines during read operations, enabling faster access times.
   - Write drivers provide the necessary current to overwrite the data in the memory cells during write operations.
4. **Column Decoder and I/O Circuitry**:
   - The column decoder selects the appropriate bitline pair based on the column address.
   - I/O circuitry handles data transfer between the memory array and the external interface.

To optimize performance and density, advanced techniques like hierarchical bitline organization, divided wordline architectures, and bank-level partitioning are often employed in large memory arrays [7, 8] (see Table 1).

**Table 1.** Standard Techniques

| Technique | Description |
|---|---|
| Hierarchical Bitline | Bitlines are divided into local and global segments, with local sense amplifiers reducing capacitive loading. |
| Divided Wordline | Wordlines are split into multiple segments, reducing wordline delay and power consumption. |
| Bank Partitioning | The array is divided into multiple banks, enabling concurrent access and improved throughput. |

These techniques, combined with innovative memory cell designs and sense amplifier architectures, contribute to the development of high-performance, energy-efficient memory subsystems in modern CMOS VLSI systems [9].

## 4. Sense Amplifiers

Sense amplifiers play a crucial role in memory arrays by detecting and amplifying the small voltage differences on the bitlines during read operations, enabling faster access times. Here are some key aspects of sense amplifiers in memory designs (see Fig. 3):

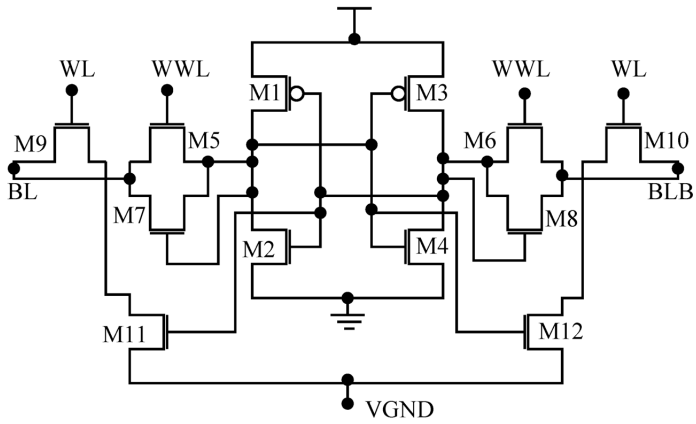


**Figure 3.** Proposed read stability and write performance aware 12T SRAM.

1. **Sense Amplifier Architecture**:
   - **Differential Sense Amplifiers**: These amplifiers detect the voltage difference between the bitline and its complementary bitline_bar, amplifying the small signal to a full logic level.
   - **Current Sense Amplifiers**: Instead of voltage sensing, these amplifiers detect the current difference between the bitlines, offering potential advantages in low-voltage operation.
2. **Sense Amplifier Placement and Organization**:
   - **Shared Sense Amplifiers**: To reduce area overhead, sense amplifiers are often shared across multiple bitline pairs through multiplexing.
   - **Hierarchical Organization**: In large arrays, sense amplifiers can be organized hierarchically, with local sense amplifiers feeding into global sense amplifiers, reducing capacitive loading and improving performance.

3. **Sense Amplifier Timing and Control**:
   - **Precharge Phase**: Before a read operation, the bitlines are precharged to a specific voltage level to enable differential sensing.
   - **Evaluation Phase**: During this phase, the sense amplifier detects and amplifies the bitline voltage difference, driving the bitlines to full logic levels.
   - **Equalization Phase**: After the read operation, the bitlines are equalized to prepare for the next cycle.
4. **Sense Amplifier Design Considerations**:
   - **Speed**: Sense amplifiers must be designed to amplify the bitline signals quickly, minimizing access time.
   - **Offset Compensation**: Techniques like auto-zeroing or digital calibration may be employed to compensate for offsets and mismatches in the sense amplifier.
   - **Power Consumption**: Sense amplifier design should balance performance and power consumption, considering factors like bitline capacitance and leakage currents.

Innovative sense amplifier architectures, such as those leveraging SiNWFET technology, can potentially offer improved performance, lower power consumption, and better scalability compared to traditional CMOS-based designs, contributing to the advancement of high-performance memory subsystems in modern CMOS VLSI systems [10, 11, 12, 13, 14].

## 5. Memory Design Shift Left

The "shift left" approach refers to the practice of moving design and verification activities earlier in the CMOS memory design process. By shifting these activities to the left (earlier) in the design flow, potential issues can be identified and addressed upfront, reducing the overall design cycle time and cost. This approach involves incorporating design for manufacturing (DFM) and design for test (DFT) considerations early on, enabling the identification and resolution of potential manufacturing and testability challenges before they become more difficult and expensive to address later in the process [15] (see Fig. 4).

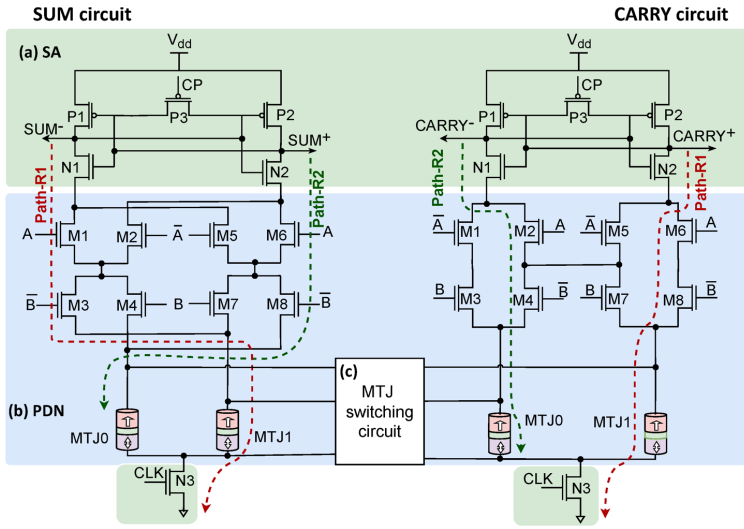


**Figure 4.** NV-FA based on IMC.

Techniques like multi-corner multi-mode (MCMM) analysis are employed to verify the design under various operating conditions and process variations. This comprehensive and rigorous verification approach helps improve the overall quality and reliability of the design. The shift left approach in CMOS memory design aims to address four key bottlenecks that impact the overall turnaround time (TAT) and time-to-market (TTM) for memory development [16, 17]:

1. Macro cell characterization
2. Block-level design optimization
3. Pre-layout to post-layout simulation gap
4. Custom layout design

The Synopsys Custom Design Family provides solutions to address these bottlenecks :

- **PrimeSim Continuum**: Addresses macro cell characterization.
- **PrimeSim Continuum and PrimeWave Design Environment**: Addresses block-level design optimization and the pre-layout to post-layout simulation gap.
- **Synopsys Custom Compiler**: Addresses custom layout design.

By leveraging these solutions and shifting the memory design and verification process to the left, TAT and TTM can be reduced while maintaining the quality of power, performance, and area (PPA) results [18] (see Fig. 5).

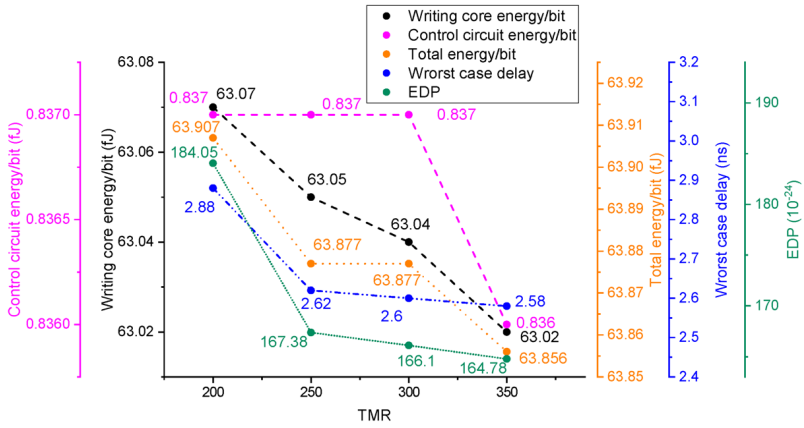


**Figure 5.** VG+SOT write circuit's performance.

Memory design shift left also involves the use of early detection tools forDRC, LVS, and ERC verification, along with automation to streamline verification processes and reduce manual intervention. Collaboration among different design teams, includingIP designers, block designers, and P&R engineers, is crucial for the success of this approach. For example:

- **IP Designers**: The shift left approach ensures signoff-clean hard IP components and enables early detection and correction of issues in soft IP, improving the efficiency of custom cell design.
- **Block Designers and P&R Engineers**: This approach helps identify issues in placements, abstracts, and layouts early, simplifying the handling of engineering change orders (ECOs) and enabling smoother integration of custom IP cells.
- **Full Chip Designers**: The shift left approach narrows down the focus for antenna checks, simplifies the implementation of design changes during final stages, and streamlines the debugging process by improving identification of changes between design revisions.

## 6. Memory Design Digitization

The digitization of memory design involves the adoption of digital techniques and methodologies to enhance various aspects of memory development, including design, verification, and optimization. This approach leverages the power of digital tools and automation to streamline processes, improve efficiency, and enable more comprehensive exploration of the design space [19, 20] (see Fig. 6).

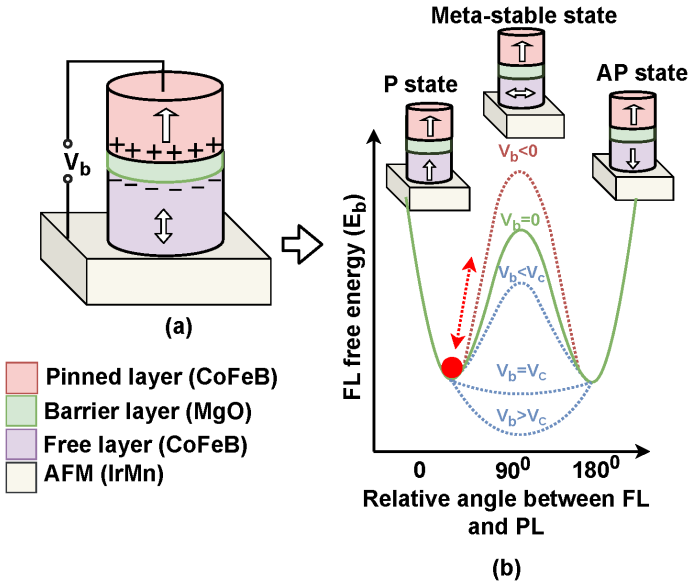


**Figure 6.** VCMA effect in VG+SOT.

1. **Digital Design Exploration**:
   - Design space exploration tools allow for the rapid evaluation of numerous memory architecture configurations, enabling the identification of optimal solutions based on performance, power, and area (PPA) requirements.
   - Automated design flows facilitate the generation and evaluation of memory compilers, reducing manual effort and accelerating the design cycle.
2. **Digital Verification**:
   - Digital verification techniques, such as formal verification and constrained-random verification, provide exhaustive coverage and enable the detection of corner-case bugs that might be missed by traditional simulation-based approaches.
   - Automated test pattern generation and fault simulation tools enhance the quality and efficiency of memory testing and verification.
3. **Digital Optimization**:
   - Digital optimization tools leverage advanced algorithms and machine learning techniques to optimize memory designs for various objectives, such as power, performance, or area.
   - These tools can explore a vast design space, considering multiple constraints and trade-offs, to identify optimal solutions that may not be apparent through manual exploration.
4. **Digital Signoff and Closure**:
   - Digital signoff tools automate the verification of memory designs against a comprehensive set of design rules, ensuring compliance with manufacturing requirements and reducing the risk of costly respins.

- Digital closure tools streamline the process of integrating memory instances into larger system-on-chip (SoC) designs, minimizing manual effort and potential errors.

5. **Digital Collaboration and Data Management**:
   - Digital collaboration platforms enable seamless communication and data sharing among geographically dispersed teams, facilitating efficient collaboration throughout the memory design process.
   - Centralized data management systems ensure version control, traceability, and secure access to design data, reducing the risk of data loss or corruption.

The digitization of memory design processes not only enhances efficiency and productivity but also enables more comprehensive exploration of the design space, leading to optimized solutions that meet stringent PPA requirements. As memory designs continue to scale and become more complex, the adoption of digital techniques and methodologies will be crucial in maintaining a competitive edge in the CMOS VLSI industry [21].

Memory designdigitization also plays a pivotal role in addressing the challenges associated with advanced technology nodes, such as process variations, reliability concerns, and design complexity. By leveraging digital tools and automation, designers can effectively analyze and mitigate these challenges, ensuring the robustness and reliability of memory designs in cutting-edge CMOS VLSI technologies [22, 23].

## 7. Reliability Challenges

Manufacturing process variations, such as random dopant fluctuations, gate material granularity, and BEOL variations, can lead to systematic and random variations in transistor characteristics. Environmental variations, like temperature and power supply noise, can also impact transistor electrical characteristics like mobility and threshold voltage. Additionally, aging and wear-out mechanisms, including Bias Temperature Instability (BTI), Hot Carrier Injection (HCI), and Electromigration (EM), can degrade transistor performance over time [24] (see Fig. 7).

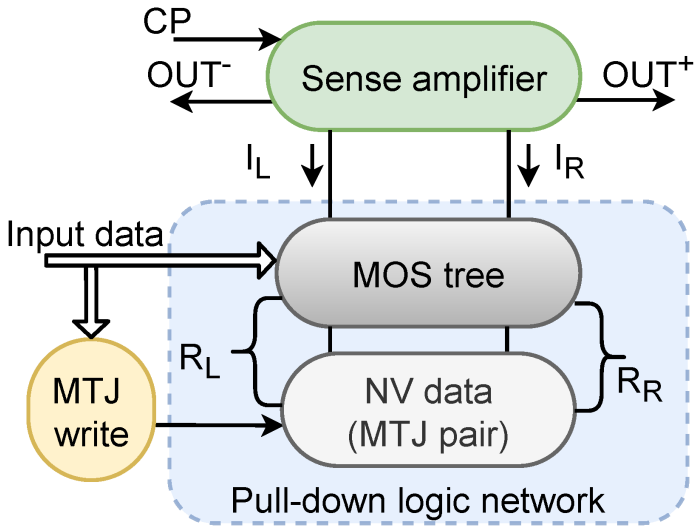


**Figure 7.** General IMC Block diagram consisting of sense amplifier.

The relationship between reliability factors and security mechanisms can be 'good, bad, and ugly',

as process variations, temperature, power supply noise, and aging/wear-out can have both positive and negative impacts on different security applications and primitives. For instance:

- Physical Unclonable Functions (PUFs) and True Random Number Generators (TRNGs) leverage process variations to generate unique signatures or random numbers.
- Detecting counterfeit/recycled electronics can utilize aging degradation as a fingerprint.

However, emerging nanodevices like Phase Change Memory (PCM) and Carbon Nanotubes (CNTs) exhibit high variability, which can be leveraged for security primitives like PUFs, but their reliability issues make them less suitable for high-performance logic applications. Therefore, there is a need to find a balance between performance, reliability, and security when designing integrated circuits [25] (see Table 2).

**Table 2.** Reliability Factors

| Reliability Factor | Impact on Security |
|---|---|
| Process Variations | Positive (PUFs, TRNGs) |
| Temperature, Power Supply Noise | Positive and Negative |
| Aging, Wear-out | Positive (Counterfeit Detection), Negative (Performance Degradation) |

Semiconductor scaling effects on microelectronics reliability prediction, qualification strategies, and derating criteria for space applications require ongoing research. Derating microelectronic devices and their critical stress parameters in aerospace applications has been a common practice to improve device reliability and extend operating life in critical missions. However, as semiconductor manufacturers generally do not publish their reliability reports, NASA needs physics-of-failure (PoF) based derating guidance for advanced scaled microelectronic technologies for long-term critical missions (see Fig. 8).

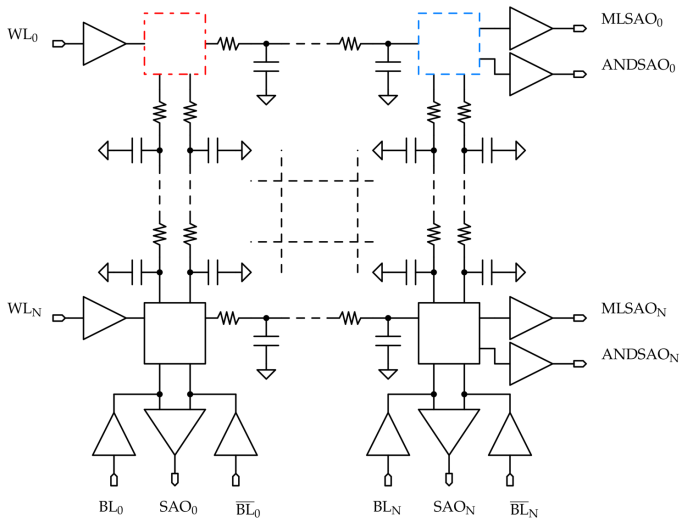


**Figure 8.** Worst case delays for each memory operation.

CMOS technology scalinghas been a primary driver of the electronics industry, but further scaling requires major changes in areas like lithography, transistor design, novel materials and structures,

and circuit sensitivity to soft errors. These challenges highlight the need for innovative solutions to ensure the reliability and security of memory designs in advanced CMOS VLSI technologies [26].

### 7.1 Reliability Solutions

To address the reliability challenges faced in advanced CMOS VLSI memory designs, several innovative solutions have been proposed and implemented. These solutions span various aspects of the design process, from device-level optimizations to system-level techniques (see Fig. 9):

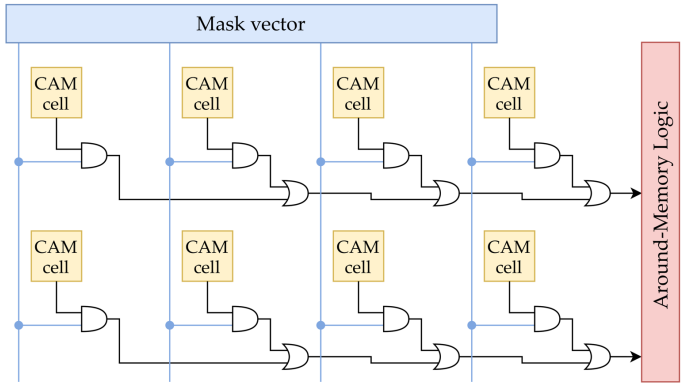


**Figure 9.** The LiM array.

1. **Device Engineering and Novel Materials**:
   - Strain engineering techniques, such as embedded SiGe source/drain stressors, can enhance carrier mobility and improve transistor performance, mitigating reliability issues like BTI and HCI.
   - The adoption of high-k metal gate (HKMG) stacks and gate-last integration schemes can reduce gate leakage currents and improve electrostatic control, enhancing reliability.
   - Novel materials like III-V compound semiconductors, carbon nanotubes, and 2D materials (e.g., graphene, MoS2) are being explored as potential replacements for silicon, offering improved performance and reliability characteristics.
2. **Circuit Design Techniques**:
   - Adaptive body biasing (ABB) and dynamic voltage and frequency scaling (DVFS) techniques can be employed to mitigate aging effects and extend the lifetime of memory circuits.
   - Redundancy techniques, such as error-correcting codes (ECC) and spare rows/columns, can be implemented to tolerate and recover from memory failures.
   - Circuit-level techniques like sense amplifier offset cancellation and bitline twisting can improve noise immunity and reduce the impact of process variations.
3. **System-Level Approaches**:
   - Advanced packaging technologies, like 2.5D and 3D integration, can mitigate reliability issues by enabling heterogeneous integration of different components (e.g., logic, memory, sensors) on a single package.
   - Intelligent memory management and wear-leveling algorithms can distribute memory accesses evenly, prolonging the lifetime of non-volatile memory technologies like flash and RRAM.
   - Built-in self-test (BIST) and self-repair mechanisms can be incorporated to enable in-field testing and repair of memory arrays, improving overall system reliability.
4. **Design Automation and Verification**:

- Reliability-aware design automation tools and methodologies can incorporate reliability constraints and optimization techniques throughout the design flow, from device-level simulations to physical implementation and verification.
- Advanced verification techniques, such as statistical static timing analysis (SSTA) and Monte Carlo simulations, can be employed to analyze the impact of process variations and aging effects on memory performance and functionality.

5. **Monitoring and Adaptive Techniques**:
   - In-situ monitoring circuits and sensors can be integrated to track aging and wear-out mechanisms, enabling adaptive techniques to mitigate their effects.
   - Machine learning and data analytics techniques can be leveraged to analyze monitoring data and predict potential failures, enabling proactive maintenance and repair actions.

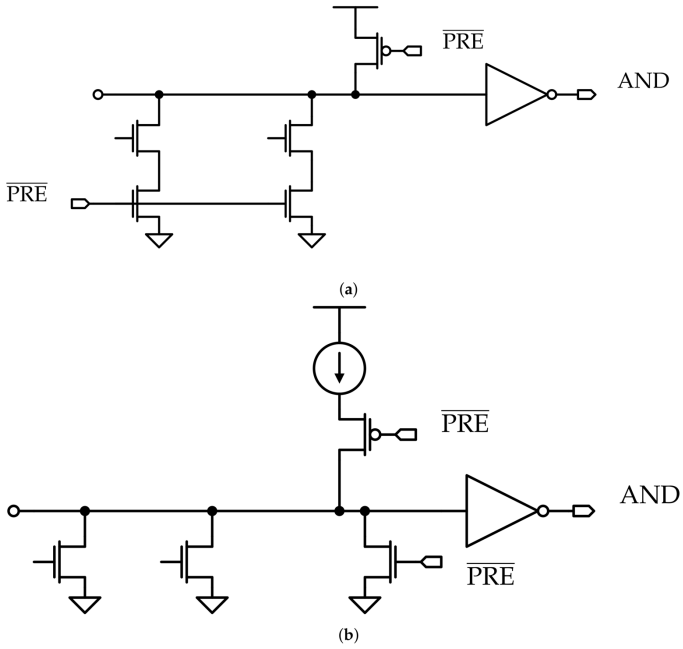


**Figure 10.** Standard and current-saving schemes.

These reliability solutions, combined with ongoing research and innovation in materials, devices, circuits, and design methodologies, aim to ensure the continued scaling and reliability of CMOS VLSI memory designs, enabling the development of high-performance, energy-efficient, and robust memory subsystems for a wide range of applications [27, 28, 29] (see Fig. 10).

### 7.2 Design Technology Co-Optimization

Design Technology Co-Optimization (DTCO) has become an essential concept in the semiconductor industry, especially for complex sub-micron processes. It involves closer collaboration between process technology development and circuit/IP design teams to optimize the design for a specific process technology. This approach helps reduce time-to-market by enabling earlier exploration of technology choices and design styles, and assessing their impact on silicon targets. Without DTCO, projects may miss schedules, leading to huge financial losses for companies [30] (see Fig. 11).

DTCO allows tuning the design for specific process performance, cost, and technology trade-offs

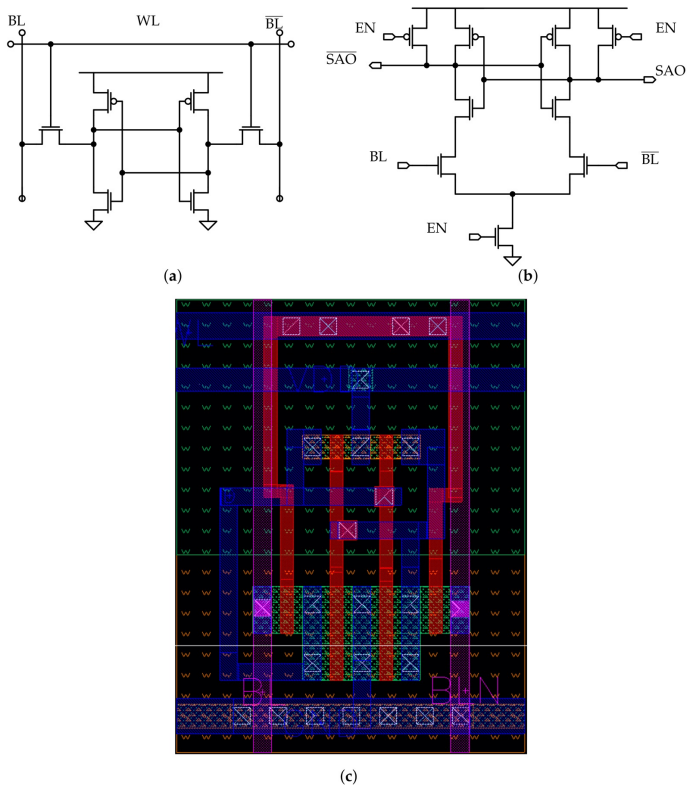


**Figure 11.** The SRAM cell and SA.

(e.g., performance, power). The process team provides design options in the form of a Process Design Kit (PDK), and the design team evaluates these PDK options to determine the best fit for their design. DTCO solutions leverage expertise across multiple domains like atomistic simulation, TCAD, lithography modeling, and design methodologies.

For example, a DTCO analysis was conducted for sub-5nm technology nodes, exploring different metal track plans, copper widths, and alternative materials like cobalt and molybdenum. This analysis helped select the optimal metal stack configuration for power and signal routing (see Table 3).

**Table 3.** DTCO Approach types

| DTCO Approach | Description |
|---|---|
| Bottom-up | DTCO enables earlier exploration of technology choices and design styles, assessing their impact on silicon targets. |
| Top-down | System-technology co-optimization (STCO) translates future system needs into technology requirements, complementing the bottom-up DTCO approach. |

STCO aims to address the right technology ingredients that can unlock major system scaling bottlenecks, such as the memory/bandwidth wall, the power/thermal wall, and the dimensional scaling wall. Imec has reorganized its core program offering to integrate all DTCO activities into one single

program that studies technology-to-circuit optimization across all core technology programs, complemented by an STCO program to translate future system needs and bottlenecks into technology requirements. While DTCO optimizes key elements of both the process and the design definition early in the technology node, the biggest challenge is that the most fundamental decisions are made with the least amount of data at the beginning of the technology development cycle. Mitigating the risk of making wrong decisions by maintaining multiple options and "downselecting" as data becomes available is cost and time prohibitive.

## 8. Conclusion

The relentless pursuit of performance and density scaling in CMOS VLSI has led to the exploration of innovative memory design techniques. From SiNWFET-based volatile and non-volatile memory cells to advanced array organizations, sense amplifiers, and design methodologies, the memory landscape is undergoing a transformation. These innovations aim to overcome the limitations of traditional approaches, enabling higher performance, lower power consumption, and improved reliability. As we push the boundaries of CMOS technology, challenges such as process variations, reliability concerns, and design complexity become increasingly prominent. However, the industry is responding with comprehensive solutions that span device engineering, circuit design techniques, system-level approaches, and design automation. By embracing design-technology co-optimization and leveraging the power of digitization, the memory design ecosystem is poised to deliver cutting-edge solutions that drive the next generation of CMOS VLSI systems.

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